

DECLARATION 100 QU

SCALE: 5-OCT-82

APPROVED BY:

DRAWN BY

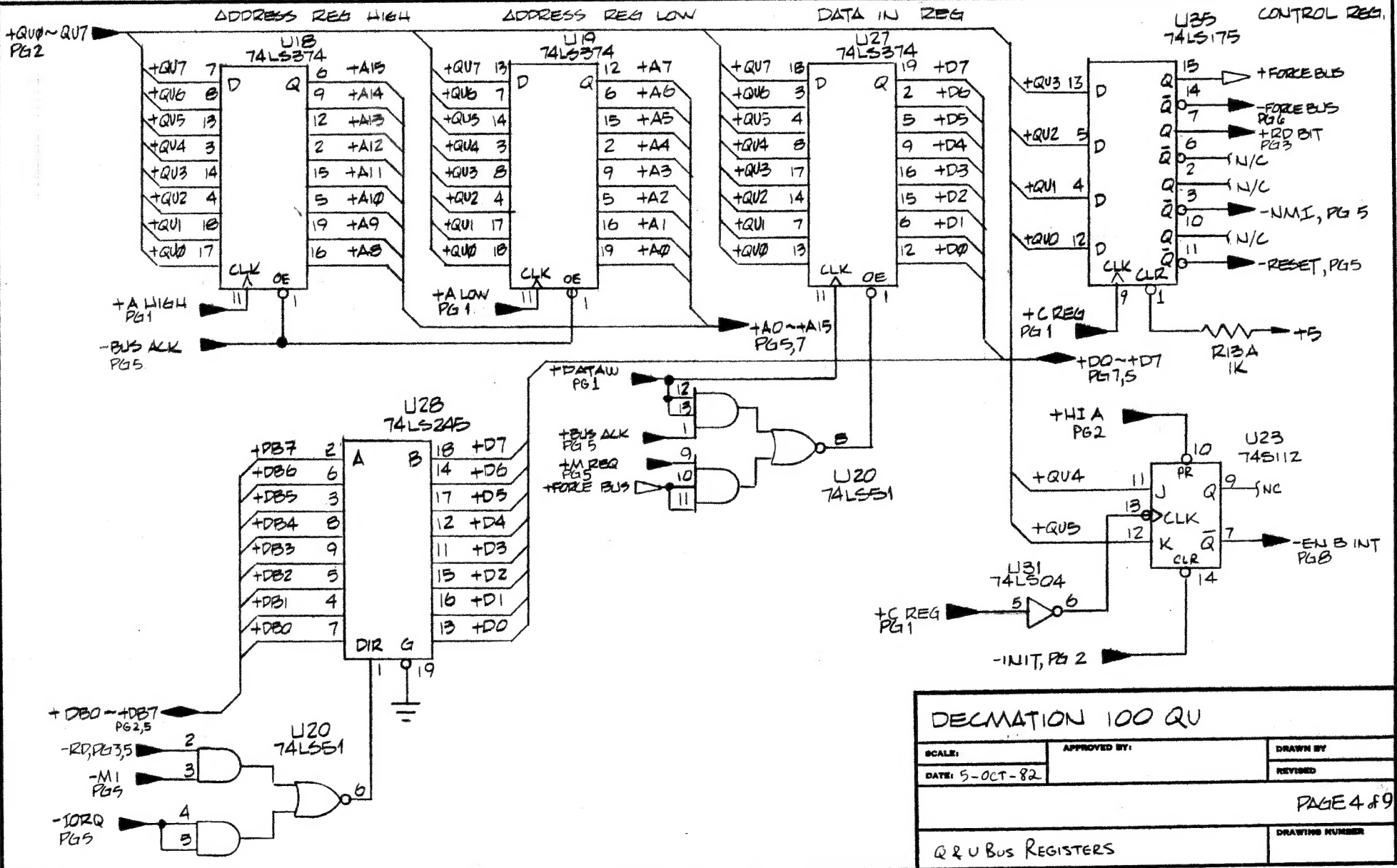
DATE:

REVISED

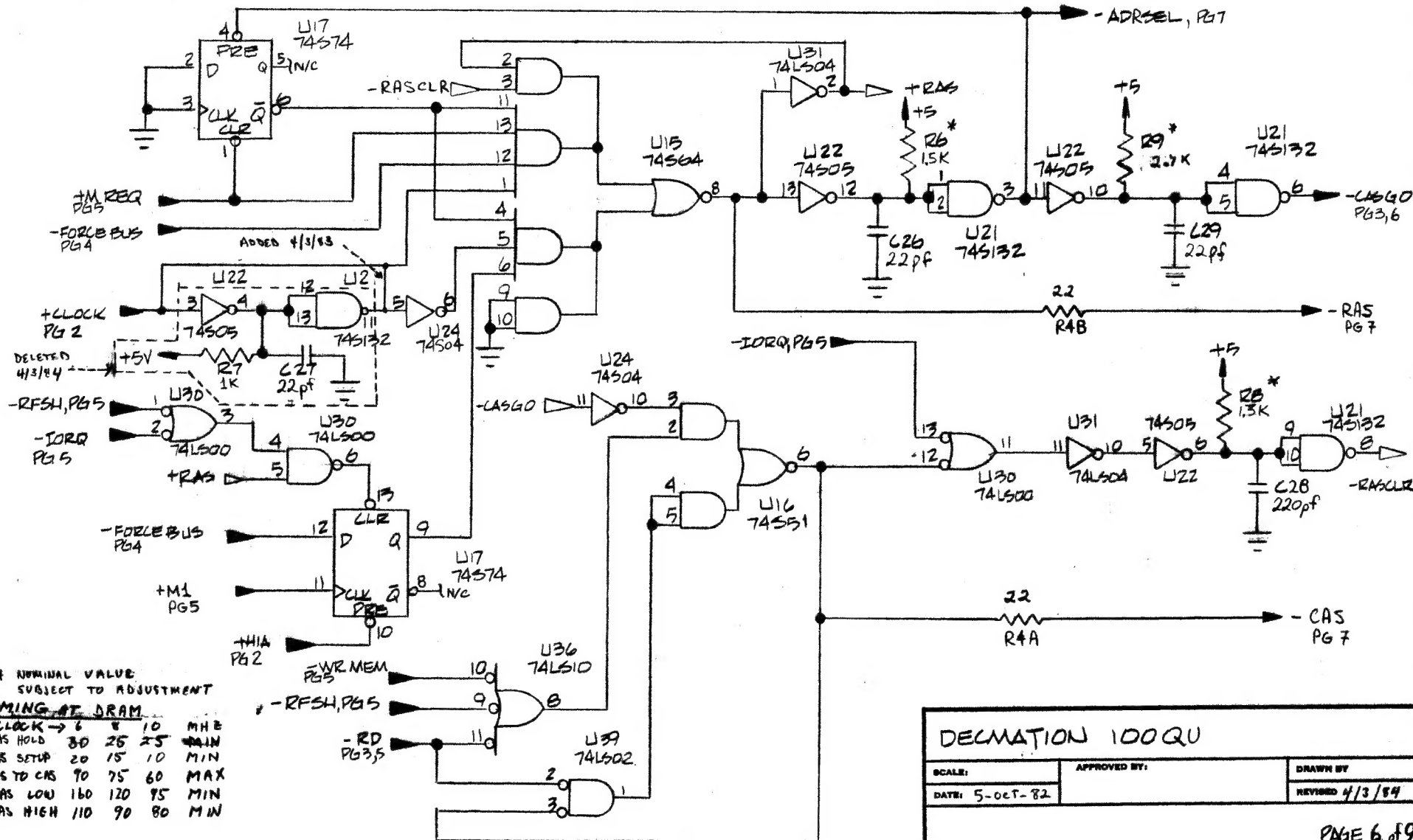
PAGE 3 of 9

DMA CONTROL LOGIC

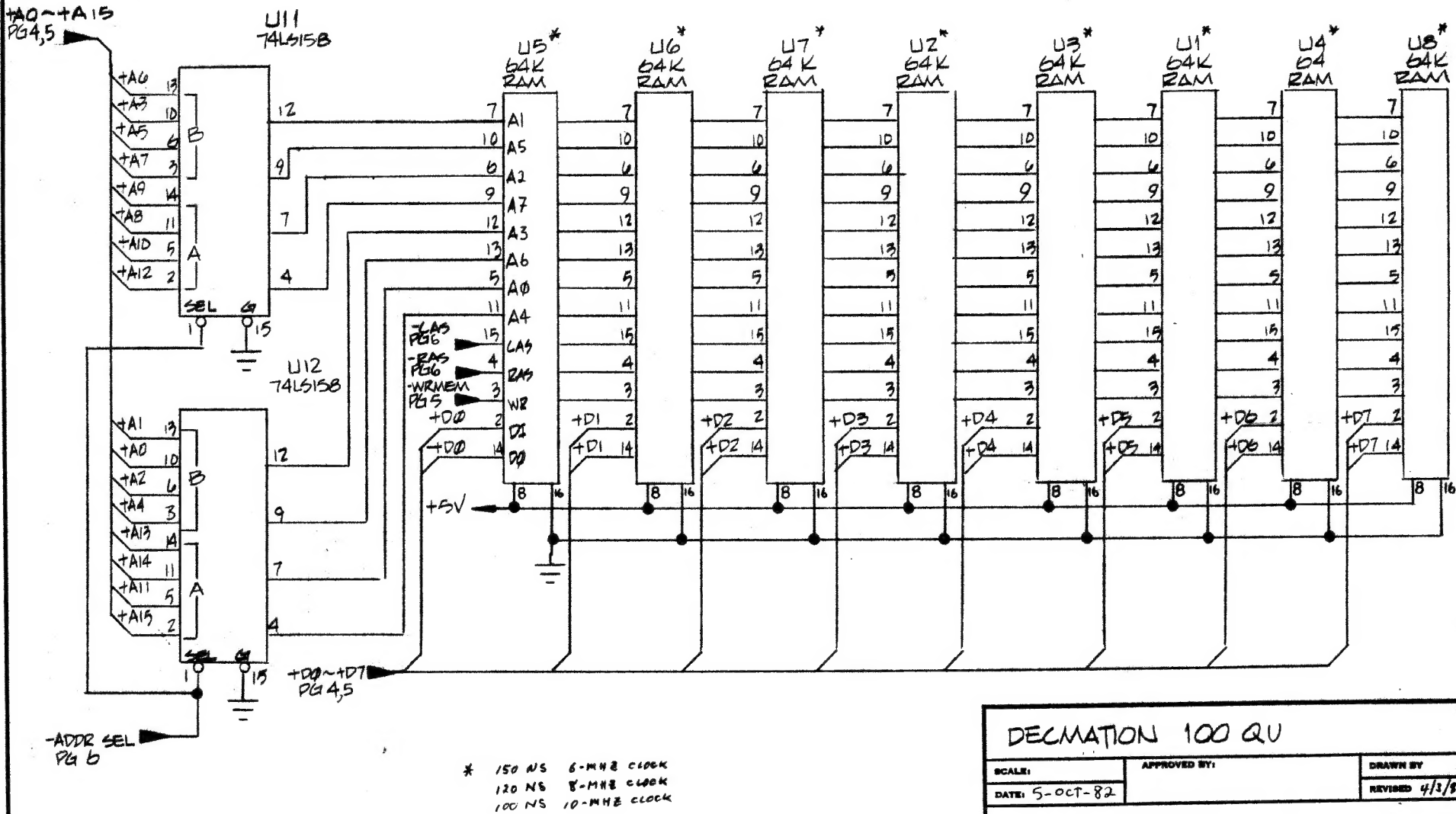
DRAWING NUMBER



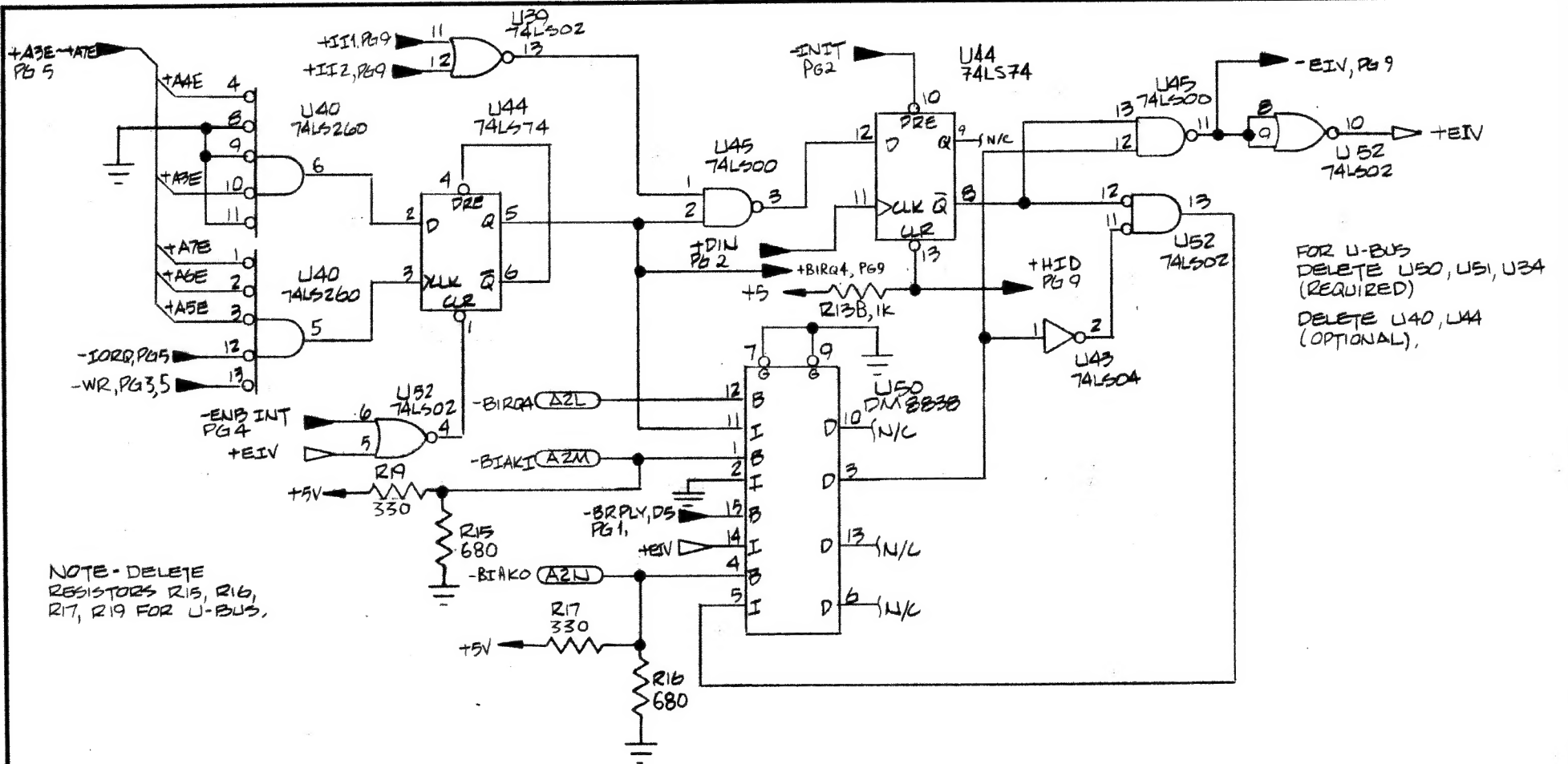
DECLAMATION 100 QU		
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DATE: 5-OCT-82		REVISED:
PAGE 4 of 9		
Q & U Bus Registers		DRAWING NUMBER:

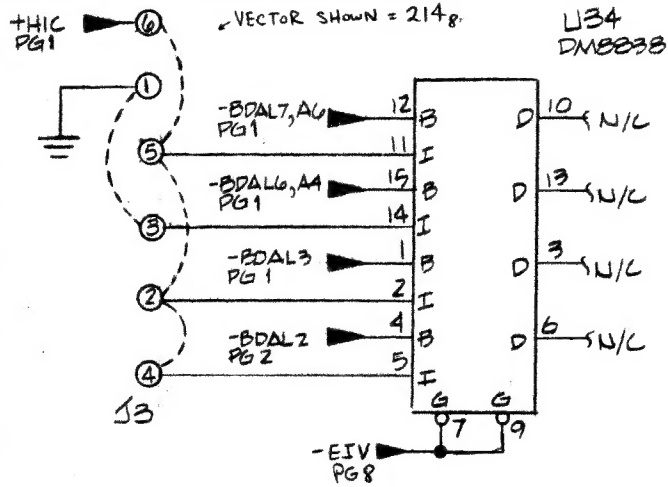


DECLARATION 100QU		
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DATE: 5-oct-82		REVISED 4/3/84
PAGE 6 of 9		
DYNAMIC RAM TIMING GENERATION		DRAWING NUMBER

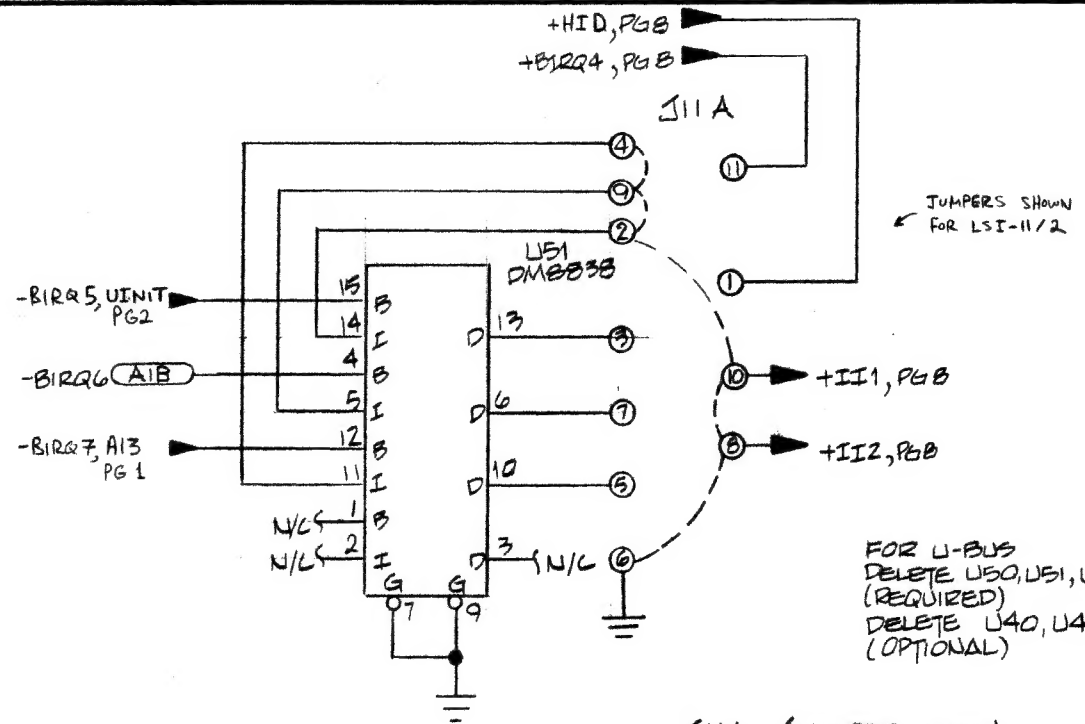


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DATE: 5-OCT-82		REVISED 4/1/84
		PAGE 7 of 9
DYNAMIC RAMS		DRAWING NUMBER





INTERRUPT VECTOR (OCTAL)	INTERRUPT VECTOR SELECTION J3 JUMPER CHAIN
100	6-3/1-2-4-5
104	6-3-4/1-2-5
110	6-3-2/1-4-5
114	6-3-2-4/1-5
200	6-5/1-2-3-4
204	6-5-4/1-2-3
210	6-5-2/1-3-4
214	6-5-4-2/1-3
300	6-3-5/1-2-4
304	6-3-5-4/1-2
310	6-3-5-2/1-4
314	6-2-3-4-5/1-N/C



J11A JUMPER CHAIN

LSI-11/2	6-2-9-4-10-8 / N.C. 5,7,3,11,1
LSI-11/23 PG1	6-2-9-4/3-10/7-8 / N.C. 5,1,11
R5	6-4-9-10/11-2/7-8 / N.C. 3,5,1
R6	6-2-4-10/11-9/5-8 / N.C. 3,7,1
R7	6-2-8-10/11-4-9 / N.C.

INTERRUPT
PRIORITY
SELECTION.

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INTERRUPT VECTOR & PRIORITY SELECT		DRAWING NUMBER

pg 9 of 9